Solo HDTC HDMI

Variant: [No Variations]

2/25/2015

V4

RELEASED - 23-JAN-2015

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for debug notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

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Title:	Solo HDTC HDMI	Variant:	[No Variations]
Page Contents:	[01] - COVER PAGE.SchDoc		Checked by
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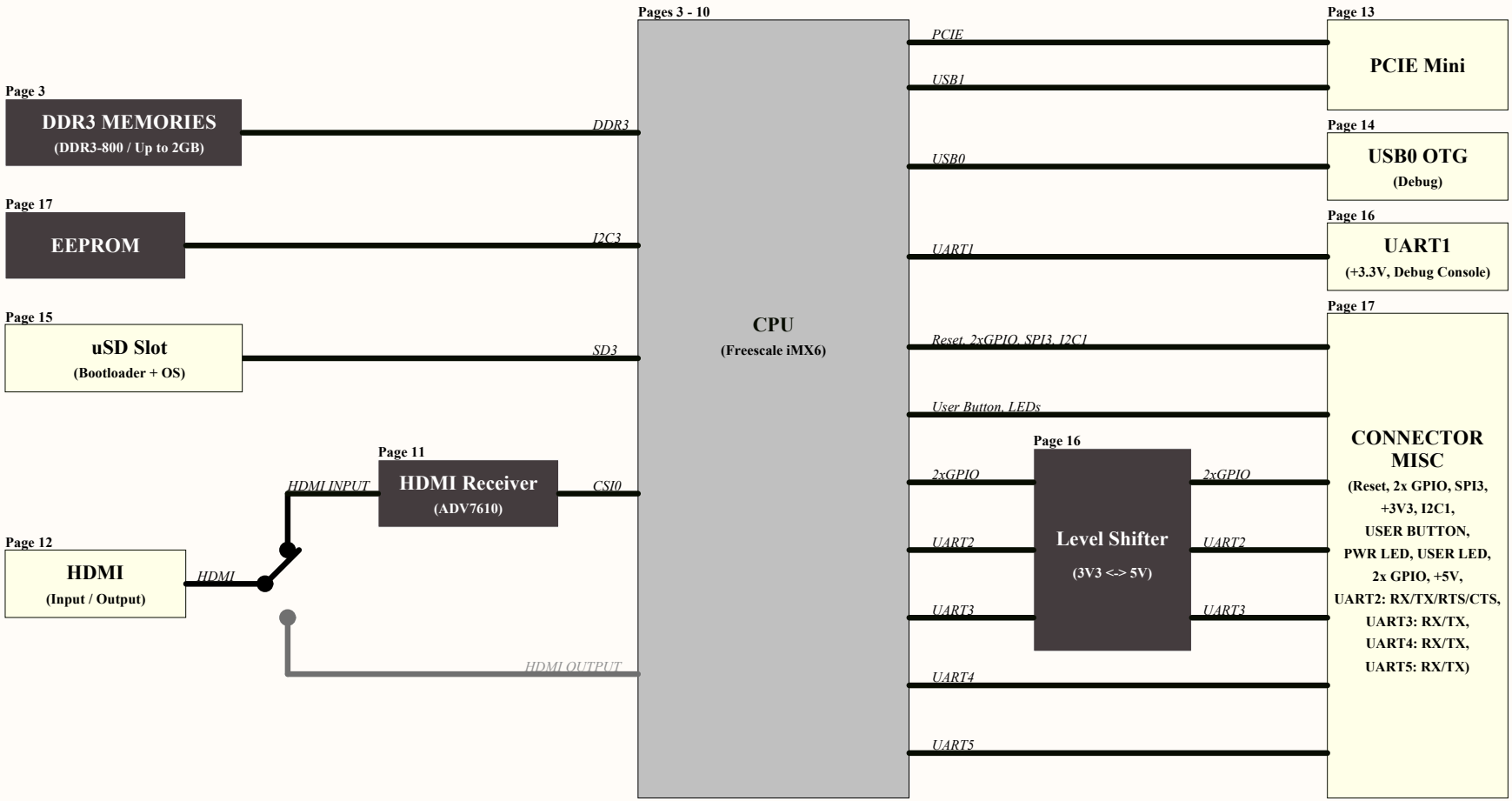
Solo HDTC HDMI

(Block Diagram)



+VIN (7~24V OR +5V)

+5V

+VIN

Page 18 — +3V3, +1V375

Page 11 — +1V8

Page 18 — +3V0 ALWAYS

Page 19 — +2V5, 1V5

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Page Contents:	[02] - BLOCK DIAGRAM.SchDoc	Checked by
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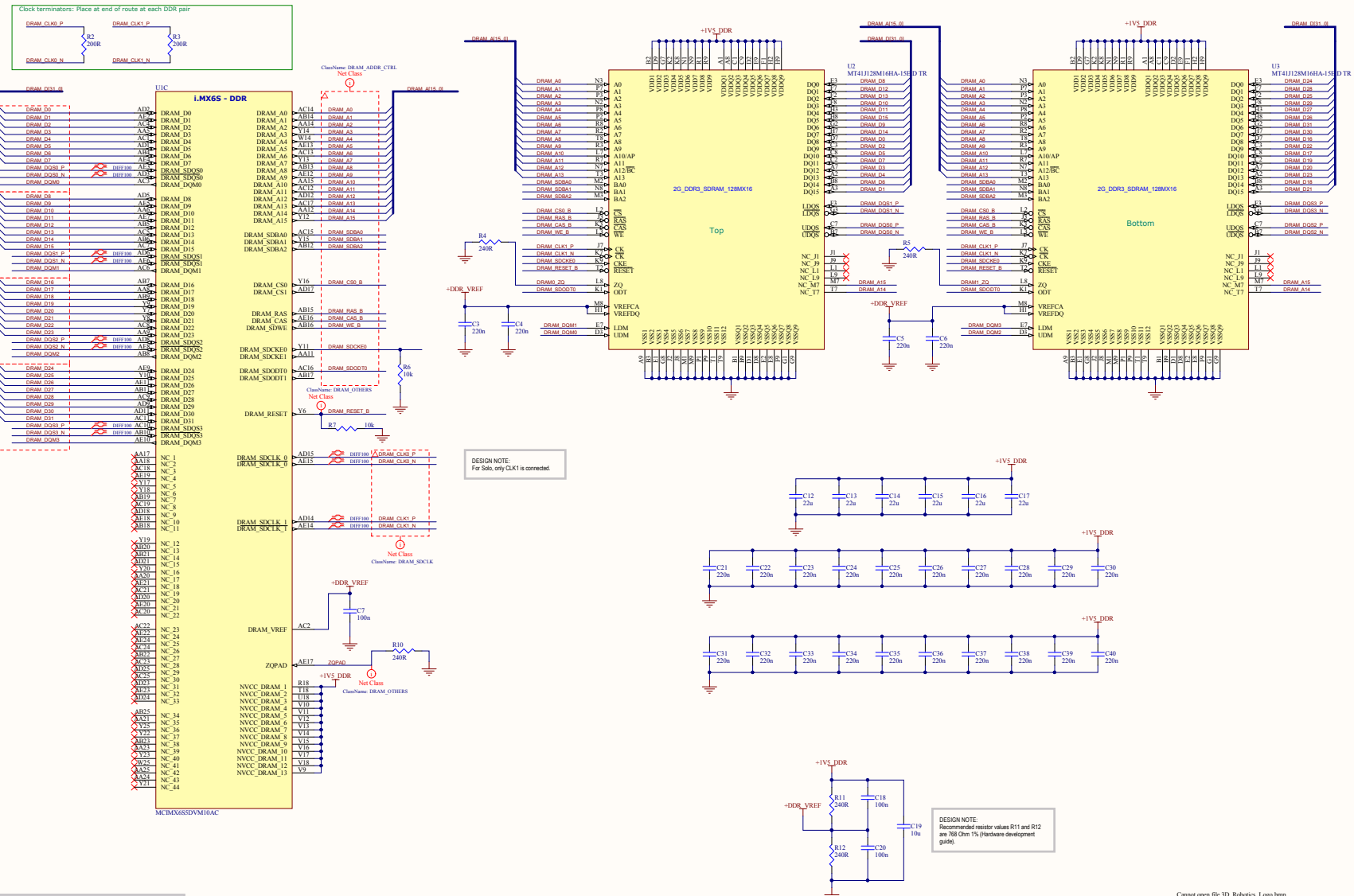
CPU - DDR3, DDR3 MEM



Title:	Solo HDTC HDMI	Variant:	[No Variations]
Page Contents:	[03] - CPU - DDR3, DDR3 MEM.SchDoc		Checked by
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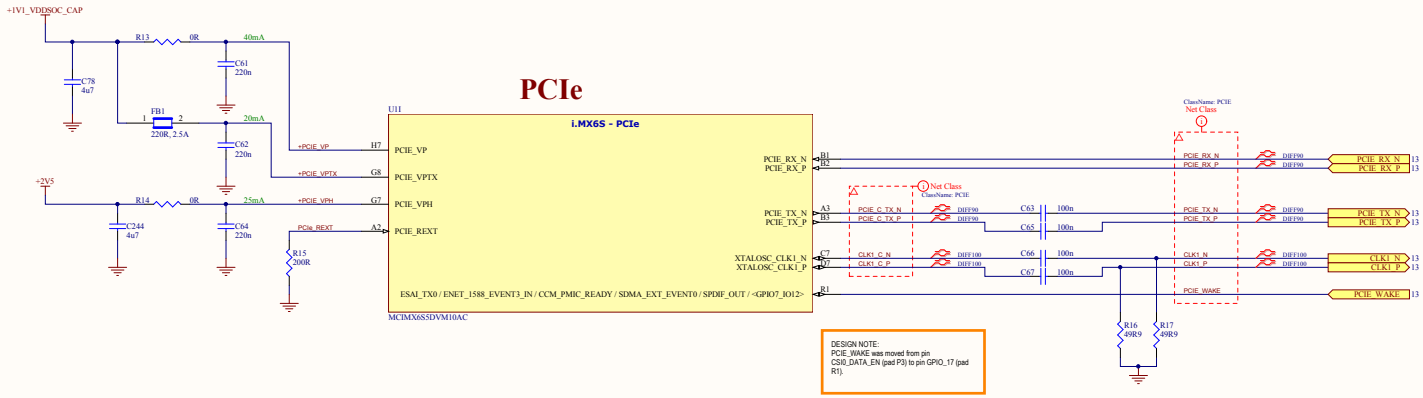
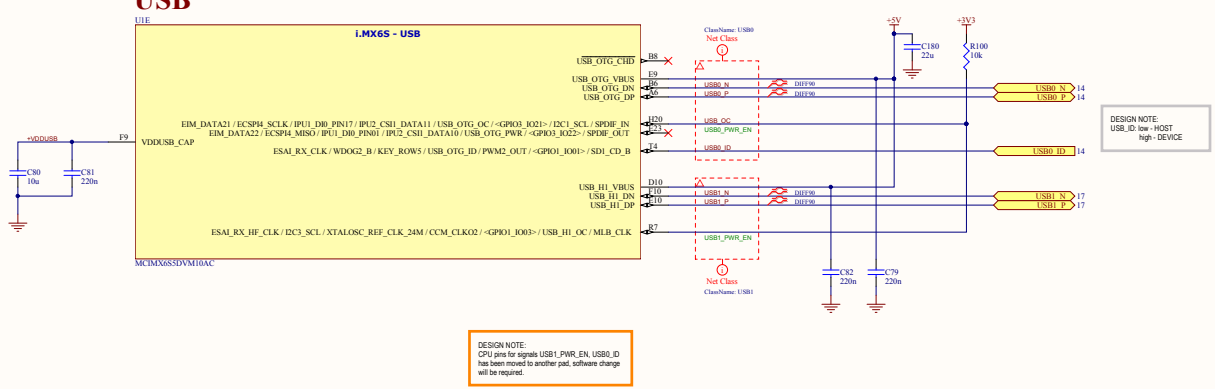
CPU - PCIE, USB

PCIe



USB



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Title:	Solo HDTC HDMI	Variant: [No Variations]
Page Contents:	[04] - CPU - PCIE, USB.SchDoc	Checked by
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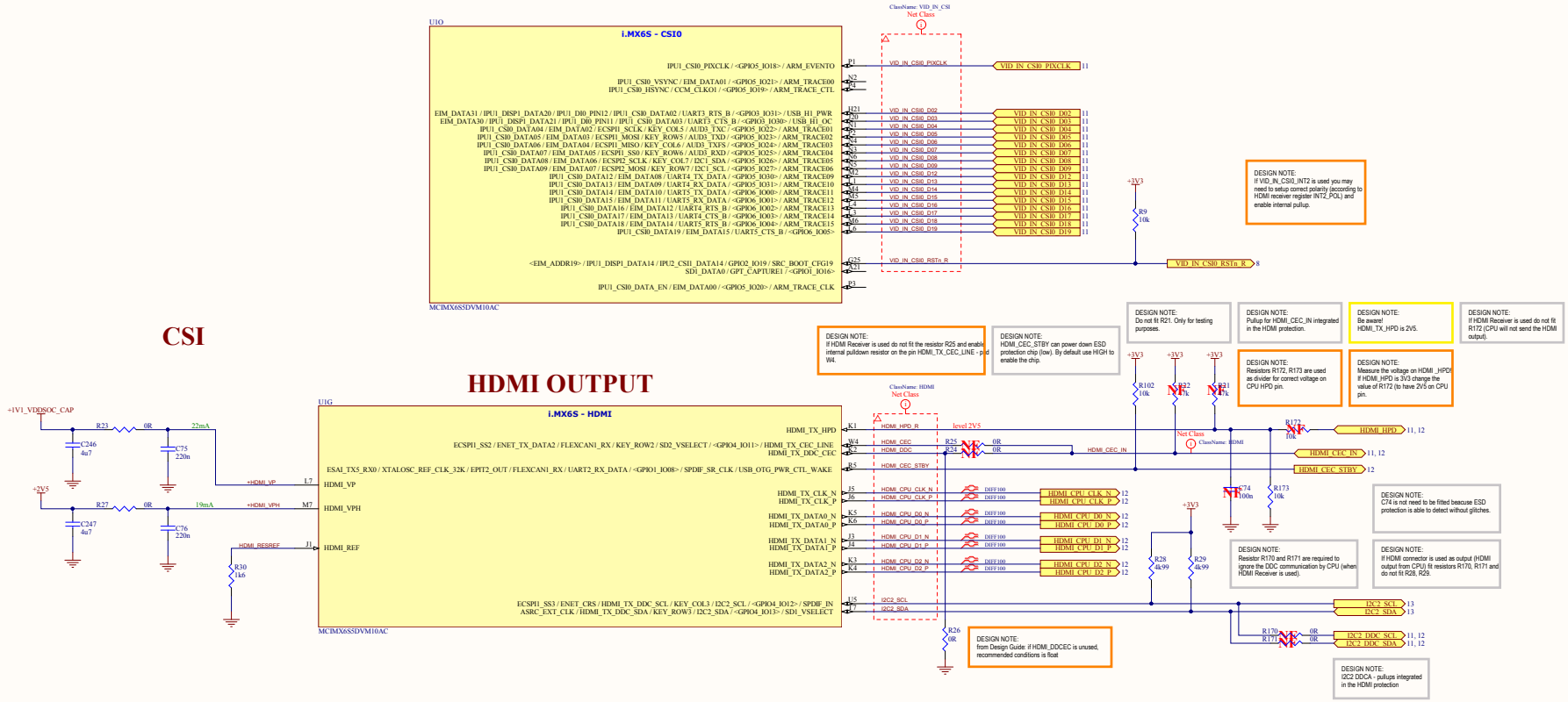
CPU - CSI, HDMI OUT

CSI

HDMI OUTPUT



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Page Contents:	[05] - CPU - CSI, HDMI OUT.SchDoc		Checked by
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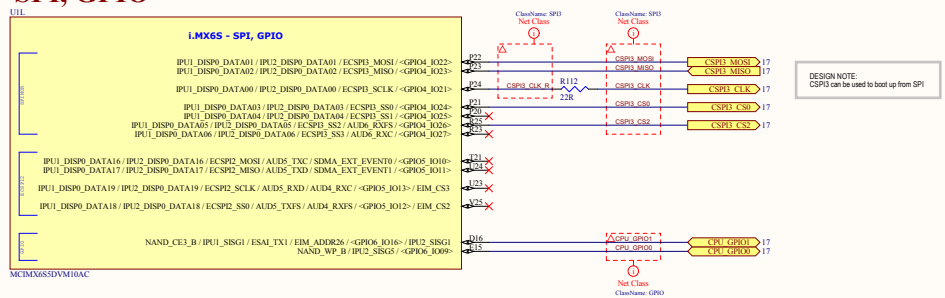
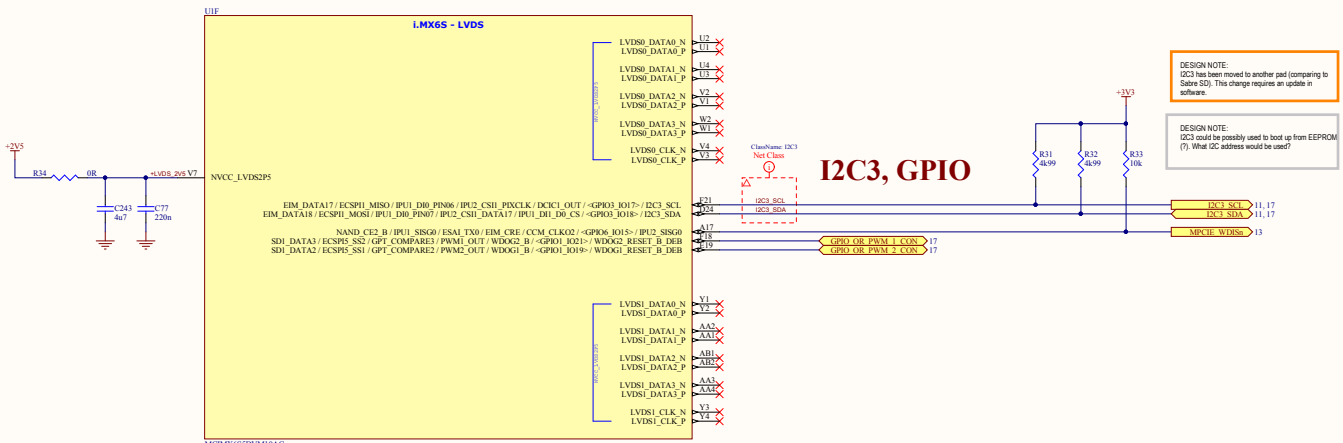
CPU - AUDIO, SPI, I2C, GPIO

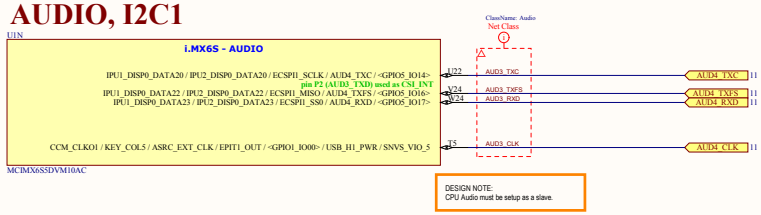
SPI, GPIO



I2C3, GPIO



AUDIO, I2C1



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Title:	Solo HDTC HDMI	Variant: [No Variations]
Page Contents:	[06] - CPU - AUDIO, SPI, I2C, GPIO.SchDoc	Checked by
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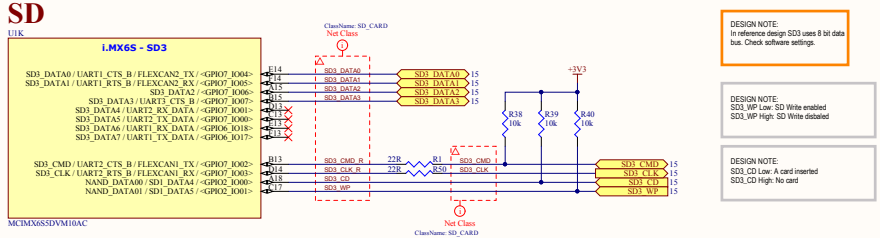
CPU - SD, UART

SD

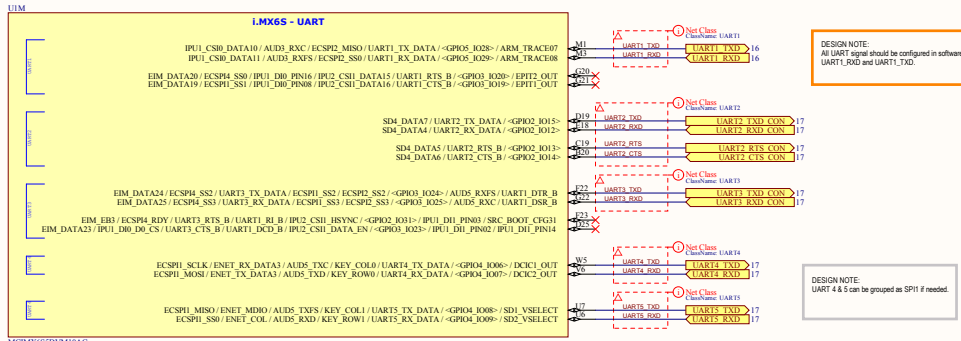


DESIGN NOTE:
In reference design SD3 uses 8 bit data bus. Check software settings.

DESIGN NOTE:
SD3_WP Low: SD Write enabled
SD3_WP High: SD Write disabled

DESIGN NOTE:
SD3_CD Low: A card inserted
SD3_CD High: No card

UART



DESIGN NOTE:
All UART signal should be configured in software except UART1_RXD and UART1_TXD.

DESIGN NOTE:
UART 4 & 5 can be grouped as SPI1 if needed.

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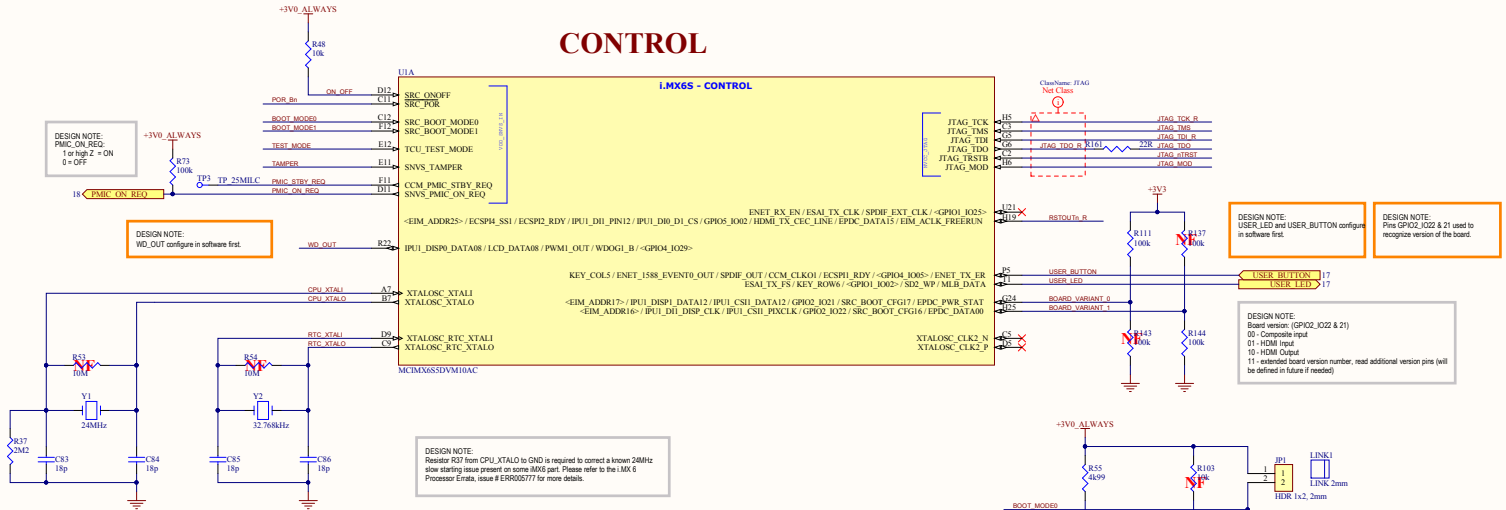
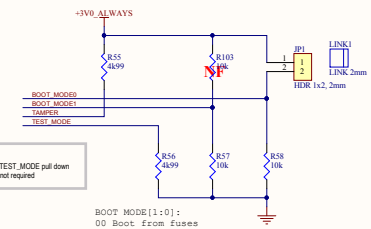
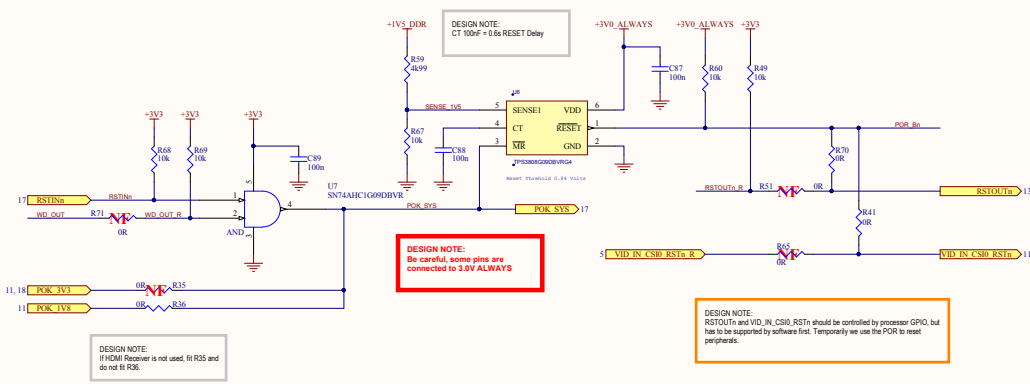
CPU - JTAG, CONTROL

CONTROL

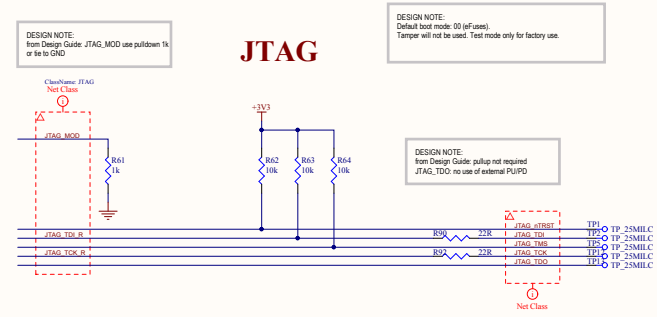




RESET



JTAG



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Title:	Solo HDTC HDMI	Variant: [No Variations]
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CPU - POWER

DESIGN NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

MX6 power domains under-BGA decoupling (belongs to CPU pins on page 4)

DESIGN NOTE:
design guide: GPANAIO must be a no connect. VDD_FA and FA_ANA should be tied to GND.

DESIGN NOTE:
Measure +1V1_NVCC_PLL_OUT, if needed fit R77, R79.

DESIGN NOTE:
+NVCC_RGMII connected to 2V5 for RGMII 2V5 operation.

DESIGN NOTE:
+NVCC_ENET connected to 2V5 to be able to easy connect cpu with ethernet phy (which is supplied from 2V5).

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CPU - UNUSED PINS

MISC

U1P

i.MX6S - UNUSED

C20 SD1_DATA1 / PWM3_OUT / GPT_CAPTURE2 / <GPIO1_IO17>
B21 SD1_CMD / ECSPI5_MOSI / PWM4_OUT / GPT_COMPARE1 / <GPIO1_IO18>
D20 SD1_CLK / ECSPI5_SCLK / GPT_CLKIN / <GPIO1_IO20>

D18 SD4_DATA0 / NAND_DQS / <GPIO2_IO08>
B19 SD4_DATA1 / PWM3_OUT / <GPIO2_IO09>
E17 SD4_DATA2 / PWM4_OUT / <GPIO2_IO10>
A20 SD4_DATA3 / <GPIO2_IO11>

B17 SD4_CMD / NAND_RE_B / UART3_TX_DATA / <GPIO7_IO09>
E18 SD4_CLK / NAND_WE_B / UART3_RX_DATA / <GPIO7_IO10>

D15 SD3_RESET / UART3_RTS_B / <GPIO7_IO08>

L20 <EIM_AD00> / IPU1_DISP1_DATA09 / IPU2_CSI1_DATA09 / GPIO3_IO00 / SRC_BOOT_CFG00
L19 <EIM_AD01> / IPU1_DISP1_DATA08 / IPU2_CSI1_DATA08 / GPIO3_IO01 / SRC_BOOT_CFG01
K20 <EIM_AD02> / IPU1_DISP1_DATA07 / IPU2_CSI1_DATA07 / GPIO3_IO02 / SRC_BOOT_CFG02
K19 <EIM_AD03> / IPU1_DISP1_DATA06 / IPU2_CSI1_DATA06 / GPIO3_IO03 / SRC_BOOT_CFG03
L18 <EIM_AD04> / IPU1_DISP1_DATA05 / IPU2_CSI1_DATA05 / GPIO3_IO04 / SRC_BOOT_CFG04
L17 <EIM_AD05> / IPU1_DISP1_DATA04 / IPU2_CSI1_DATA04 / GPIO3_IO05 / SRC_BOOT_CFG05
K18 <EIM_AD06> / IPU1_DISP1_DATA03 / IPU2_CSI1_DATA03 / GPIO3_IO06 / SRC_BOOT_CFG06
L16 <EIM_AD07> / IPU1_DISP1_DATA02 / IPU2_CSI1_DATA02 / GPIO3_IO07 / SRC_BOOT_CFG07

L24 <EIM_AD08> / IPU1_DISP1_DATA01 / IPU2_CSI1_DATA01 / GPIO3_IO08 / SRC_BOOT_CFG08
M24 <EIM_AD09> / IPU1_DISP1_DATA00 / IPU2_CSI1_DATA00 / GPIO3_IO09 / SRC_BOOT_CFG09
M23 <EIM_AD10> / IPU1_DI1_PIN15 / IPU2_CSI1_DATA_EN / GPIO3_IO10 / SRC_BOOT_CFG10
M22 <EIM_AD11> / IPU1_DI1_PIN02 / IPU2_CSI1_HSYNC / GPIO3_IO11 / SRC_BOOT_CFG11
M21 <EIM_AD12> / IPU1_DI1_PIN03 / IPU2_CSI1_VSYNC / GPIO3_IO12 / SRC_BOOT_CFG12
M20 <EIM_AD13> / IPU1_DI1_D0_CS / GPIO3_IO13 / SRC_BOOT_CFG13
N24 <EIM_AD14> / IPU1_DI1_D1_CS / GPIO3_IO14 / SRC_BOOT_CFG14
N23 <EIM_AD15> / IPU1_DI1_PIN01 / IPU1_DI1_PIN04 / GPIO3_IO15 / SRC_BOOT_CFG15

J22 <EIM_ADDR18> / IPU1_DISP1_DATA13 / IPU2_CSI1_DATA13 / GPIO2_IO20 / SRC_BOOT_CFG18

H22 <EIM_ADDR20> / IPU1_DISP1_DATA15 / IPU2_CSI1_DATA15 / GPIO2_IO18 / SRC_BOOT_CFG20
H23 <EIM_ADDR21> / IPU1_DISP1_DATA16 / IPU2_CSI1_DATA16 / GPIO2_IO17 / SRC_BOOT_CFG21
G24 <EIM_ADDR22> / IPU1_DISP1_DATA17 / IPU2_CSI1_DATA17 / GPIO2_IO16 / SRC_BOOT_CFG22
F24 <EIM_ADDR23> / IPU1_DISP1_DATA18 / IPU2_CSI1_DATA18 / IPU2_SISG3 / IPU1_SISG3 / GPIO6_IO06 / SRC_BOOT_CFG23
F23 <EIM_ADDR24> / IPU1_DISP1_DATA19 / IPU2_CSI1_DATA19 / IPU2_SISG2 / IPU1_SISG2 / GPIO5_IO04 / SRC_BOOT_CFG24

C22 EIM_DATA16 / ECSPI1_SCLK / IPU1_DI0_PIN05 / IPU2_CSI1_DATA18 / HDMI_TX_DDC_SDA / <GPIO3_IO16> / I2C2_SDA

E24 EIM_DATA26 / IPU1_DI1_PIN11 / IPU1_CSI0_DATA01 / IPU2_CSI1_DATA14 / UART2_TX_DATA / <GPIO3_IO26> / IPU1_SISG2 / IPU1_DISP1_DATA22
E23 EIM_DATA27 / IPU1_DI1_PIN13 / IPU1_CSI0_DATA00 / IPU2_CSI1_DATA13 / UART2_RX_DATA / <GPIO3_IO27> / IPU1_SISG3 / IPU1_DISP1_DATA23
D24 EIM_DATA28 / I2C1_SDA / ECSPI4_MOSI / IPU2_CSI1_DATA12 / UART2_CTS_B / <GPIO3_IO28> / IPU1_EXT_TRIG / IPU1_DI0_PIN13
J18 EIM_DATA29 / IPU1_DI1_PIN15 / ECSPI4_SS0 / UART2_RTS_B / <GPIO3_IO29> / IPU2_CSI1_VSYNC / IPU1_DI0_PIN14

N22 <EIM_BCLK> / IPU1_DI1_PIN16 / GPIO6_IO31
T23 <EIM_LBA> / IPU1_DI1_PIN17 / ECSPI2_SS1 / GPIO2_IO27 / SRC_BOOT_CFG26
T22 <EIM_OE> / IPU1_DI1_PIN07 / ECSPI2_MISO / GPIO2_IO25
K24 <EIM_RW> / IPU1_DI1_PIN08 / ECSPI2_SS0 / GPIO2_IO26 / SRC_BOOT_CFG29
M19 <EIM_WAIT> / EIM_DTACK_B / GPIO5_IO00 / SRC_BOOT_CFG25

K21 <EIM_EB0> / IPU1_DISP1_DATA11 / IPU2_CSI1_DATA11 / CCM_PMIC_READY / GPIO2_IO28 / SRC_BOOT_CFG27
K23 <EIM_EB1> / IPU1_DISP1_DATA10 / IPU2_CSI1_DATA10 / GPIO2_IO29 / SRC_BOOT_CFG28
E22 EIM_EB2 / ECSPI1_SS0 / IPU2_CSI1_DATA19 / HDMI_TX_DDC_SCL / <GPIO2_IO30> / I2C2_SCL / SRC_BOOT_CFG30

H24 <EIM_CS0> / IPU1_DI1_PIN05 / ECSPI2_SCLK / GPIO2_IO23
H21 <EIM_CS1> / IPU1_DI1_PIN06 / ECSPI2_MOSI / GPIO2_IO24

W20 MLB_CLK / ENET_TX_DATA1 / ESAI_TX2_RX3 / ENET_1588_EVENT0_IN / <GPIO1_IO29>

P6 ESAI_TX1 / ENET_RX_CLK / SD3_VSELECT / SDMA_EXT_EVENT1 / ASRC_EXT_CLK / <GPIO7_IO13> / SNVS_VIO_5_CTL
R5 ESAI_TX2_RX3 / KEY_ROW7 / CCM_CLKO1 / <GPIO1_IO05> / I2C3_SCL / ARM_EVENTI
P5 ESAI_TX3_RX2 / ENET_1588_EVENT2_IN / ENET_REF_CLK / SD1_LCTL / SPDIF_IN / <GPIO7_IO11> / I2C3_SDA / JTAG_DE_B
P4 ESAI_TX4_RX1 / ECSPI5_RDY / EPIT1_OUT / FLEXCAN1_TX / UART2_TX_DATA / <GPIO1_IO07> / SPDIF_LOCK / USB_OTG_HOST_MODE

R6 ESAI_TX_HF_CLK / KEY_COL7 / <GPIO1_IO04> / SD2_CD_B
T5 ESAI_RX_FS / WDOG1_B / KEY_COL6 / CCM_REF_EN_B / PWM1_OUT / <GPIO1_IO09> / SD1_WP

W23 USB_OTG_ID / ENET_RX_ER / ESAI_RX_HF_CLK / SPDIF_IN / ENET_1588_EVENT2_OUT / <GPIO1_IO24>
W24 ENET_RX_DATA0 / ESAI_TX_HF_CLK / SPDIF_OUT / <GPIO1_IO27>
U24 ECSPI1_SS1 / ENET_RX_DATA2 / FLEXCAN1_TX / KEY_COL2 / ENET_MDC / <GPIO4_IO10> / USB_H1_PWR_CTL_WAKE
V24 ENET_TX_DATA0 / ESAI_TX4_RX1 / <GPIO1_IO30>

T6 FLEXCAN2_TX / IPU1_SISG4 / USB_OTG_OC / KEY_COL4 / UART5_RTS_B / <GPIO4_IO14>
V5 FLEXCAN2_RX / IPU1_SISG5 / USB_OTG_PWR / KEY_ROW4 / UART5_CTS_B / <GPIO4_IO15>

IPU1_DI0_PIN02 / IPU2_DI0_PIN02 / AUD6_TXD / <GPIO4_IO18> N25
IPU1_DI0_PIN03 / IPU2_DI0_PIN03 / AUD6_TXFS / <GPIO4_IO19> P20
IPU1_DI0_PIN04 / IPU2_DI0_PIN04 / AUD6_RXD / SD1_WP / <GPIO4_IO20> P25
IPU1_DI0_PIN15 / IPU2_DI0_PIN15 / AUD6_TXC / <GPIO4_IO17> P21
IPU1_DI0_DISP_CLK / IPU2_DI0_DISP_CLK / <GPIO4_IO16> N19

IPU1_DISP0_DATA07 / IPU2_DISP0_DATA07 / ECSPI3_RDY / <GPIO4_IO28> R24

IPU1_DISP0_DATA09 / IPU2_DISP0_DATA09 / PWM2_OUT / WDOG2_B / <GPIO4_IO30> R25
IPU1_DISP0_DATA10 / IPU2_DISP0_DATA10 / <GPIO4_IO31> P23
IPU1_DISP0_DATA11 / IPU2_DISP0_DATA11 / <GPIO5_IO05> P24
IPU1_DISP0_DATA12 / IPU2_DISP0_DATA12 / <GPIO5_IO06> N20
IPU1_DISP0_DATA13 / IPU2_DISP0_DATA13 / AUD5_RXFS / <GPIO5_IO07> N25
IPU1_DISP0_DATA14 / IPU2_DISP0_DATA14 / AUD5_RXC / <GPIO5_IO08> N22
IPU1_DISP0_DATA15 / IPU2_DISP0_DATA15 / ECSPI1_SS1 / ECSPI2_SS1 / <GPIO5_IO09> P22

IPU1_DISP0_DATA21 / IPU2_DISP0_DATA21 / ECSPI1_MOSI / AUD4_TXD / <GPIO5_IO15> T20

NAND_CE0_B / <GPIO6_IO11> L15
NAND_CE1_B / SD4_VSELECT / SD3_VSELECT / <GPIO6_IO14> L16

NAND_ALE / SD4_RESET / <GPIO6_IO08> A16
NAND_CLE / IPU2_SISG4 / <GPIO6_IO07> B15
NAND_READY / IPU2_DI0_PIN01 / <GPIO6_IO10> B16

MLB_SIG_N A9
MLB_SIG_P B9

MLB_DATA_N B10
MLB_DATA_P A10

MLB_CLK_N A11
MLB_CLK_P B11

CSI_DATA0_N E4
CSI_DATA0_P F4

CSI_DATA1_N D1
CSI_DATA1_P D2

CSI_DATA2_N E1
CSI_DATA2_P F1

CSI_DATA3_N F2
CSI_DATA3_P F3

CSI_CLK0_N F4
CSI_CLK0_P F5

CSI_REXT D4

DSI_DATA0_N G2
DSI_DATA0_P G1

DSI_DATA1_N H2
DSI_DATA1_P H1

DSI_CLK0_N H3
DSI_CLK0_P H4

DSI_REXT G4

MCIMX6S5DVM10AC

SATA

U1D

i.MX6S - NC (SATA)

+1V1_VDDSOC_CAP
R18 0R 11mA
C68 220n
+SATA_VP G13
NC_46
+2V5
R19 0R 13mA +SATA_VPH G12
C245 4u7
C73 220n
NC_47
NC_48 A14
NC_49 B14
NC_50 B12
NC_51 A12
NC_52 C14 SATA_REXT
R20 191R

MCIMX6S5DVM10AC

DESIGN NOTE:
Freescale feedback about Solo: SATA_VP and SATA_VPH pins - these supplies should be powered if performing boundary scan tests.

ETHERNET

U1H

i.MX6S - RGMII

USB_H2_DATA / RGMII_TXC / SPDIF_EXT_CLK / <GPIO6_IO19> / XTALOSC_REF_CLK_24M D21

HSI_TX_READY / RGMII_TD0 / <GPIO6_IO20> C22
HSI_RX_FLAG / RGMII_TD1 / <GPIO6_IO21> E20
HSI_RX_DATA / RGMII_TD2 / <GPIO6_IO22> E21
HSI_RX_WAKE / RGMII_TD3 / <GPIO6_IO23> A24

USB_H2_STROBE / RGMII_TX_CTL / <GPIO6_IO26> / ENET_REF_CLK C23

USB_H3_STROBE / RGMII_RXC / <GPIO6_IO30> B25

HSI_RX_READY / RGMII_RD0 / <GPIO6_IO25> C24
HSI_TX_FLAG / RGMII_RD1 / <GPIO6_IO27> B23
HSI_TX_DATA / RGMII_RD2 / <GPIO6_IO28> H24
HSI_TX_WAKE / RGMII_RD3 / <GPIO6_IO29> D23

USB_H3_DATA / RGMII_RX_CTL / <GPIO6_IO24> D22

MLB_DATA / ENET_MDC / ESAI_TX5_RX0 / ENET_1588_EVENT1_IN / <GPIO1_IO31> V20
ENET_MDIO / ESAI_RX_CLK / ENET_1588_EVENT1_OUT / <GPIO1_IO22> / SPDIF_LOCK V23

ENET_TX_CLK / ESAI_RX_FS / <GPIO1_IO23> / SPDIF_SR_CLK V22
ENET_TX_EN / ESAI_TX3_RX2 / <GPIO1_IO28> V21
MLB_SIG / ENET_RX_DATA1 / ESAI_TX_FS / ENET_1588_EVENT3_OUT / <GPIO1_IO26> W22

MCIMX6S5DVM10AC

MMC-CARD

U1J

i.MX6S - SD2

SD2_DATA0 / ECSPI5_MISO / AUD4_RXD / KEY_ROW7 / <GPIO1_IO15> / DCIC2_OUT A22
SD2_DATA1 / ECSPI5_SS0 / EIM_CS2 / AUD4_TXFS / KEY_COL7 / <GPIO1_IO14> B20
SD2_DATA2 / ECSPI5_SS1 / EIM_CS3 / AUD4_TXD / KEY_ROW6 / <GPIO1_IO13> C21
SD2_DATA3 / ECSPI5_SS3 / KEY_COL6 / AUD4_TXC / <GPIO1_IO12> A21
NAND_DATA04 / SD2_DATA4 / <GPIO2_IO04> A10
NAND_DATA05 / SD2_DATA5 / <GPIO2_IO05> B18
NAND_DATA06 / SD2_DATA6 / <GPIO2_IO06> A17
NAND_DATA07 / SD2_DATA7 / <GPIO2_IO07> A18

SD2_CMD / ECSPI5_MOSI / KEY_ROW5 / AUD4_RXC / <GPIO1_IO11> E19
SD2_CLK / ECSPI5_SCLK /KEY_COL5 / AUD4_RXFS / <GPIO1_IO10> C17
NAND_DATA02 / SD1_DATA6 / <GPIO2_IO02> A16
NAND_DATA03 / SD1_DATA7 / <GPIO2_IO03> D17

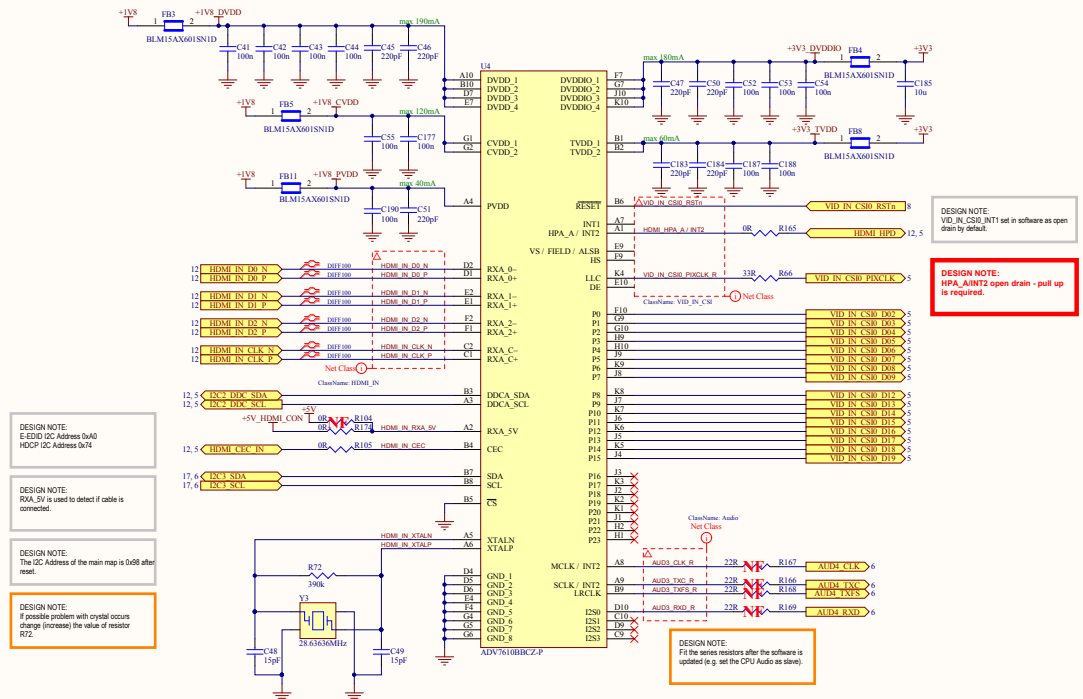
ESAI_TX_CLK / I2C3_SDA / <GPIO1_IO06> / SD2_LCTL / MLB_SIG J3

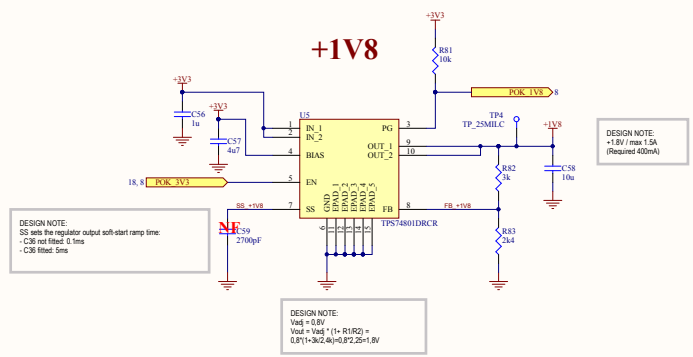
MCIMX6S5DVM10AC

Cannot open file 3D_Robotics_Logo.bmp

Title:	Solo HDTC HDMI	Variant:	[No Variations]
Page Contents:	[10] - CPU - UNUSED.SchDoc		Checked by
Size:	DWG NO	Revision:	V4
Date:	2/25/2015	Sheet	10 of 23

HDMI Input





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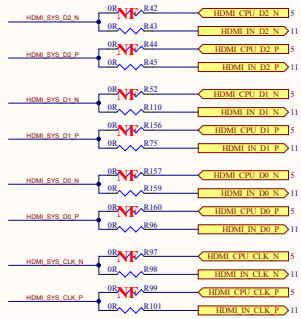
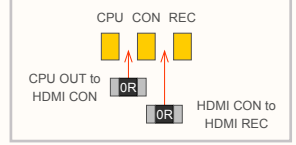
Title:	Solo HDTC HDMI
Variant:	[No Variations]
Page Contents:	[11] - HDMI INPUT.SchDoc
Checked by	
Size:	DWG NO
Revision:	V4
Date:	2/25/2015
Sheet	11 of 23

HDMI, HDMI Output

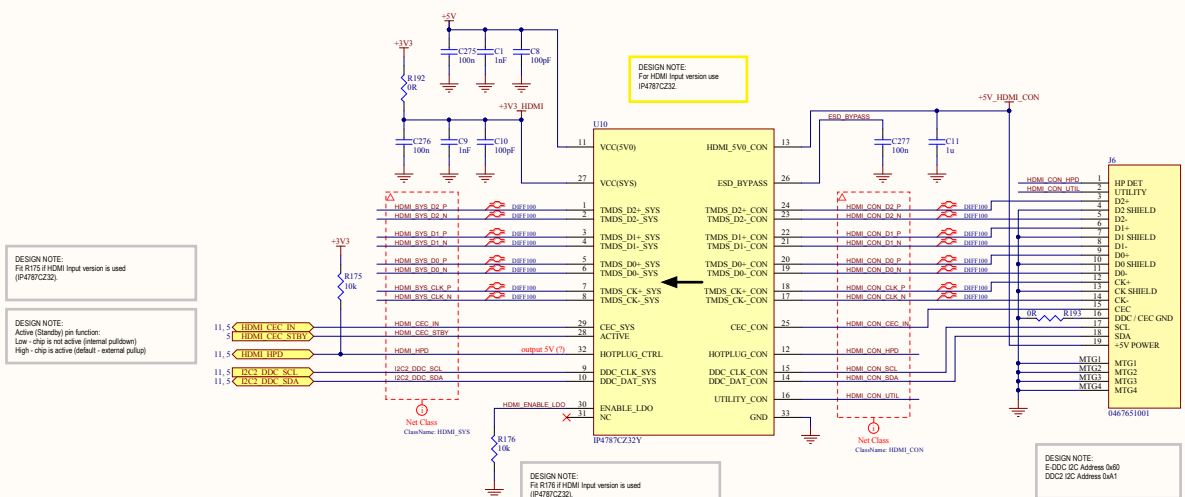
HDMI Routing



DESIGN NOTE:
Fit only one resistor per signal according to the picture below.



HDMI Connector



DESIGN NOTE:
For HDMI Input version use IP4787CZ32.

DESIGN NOTE:
Fit R175 if HDMI Input version is used (IP4787CZ32).

DESIGN NOTE:
Active (Standby) pin function:
Low - chip is not active (internal pulldown)
High - chip is active (default - external pullup)

DESIGN NOTE:
Fit R176 if HDMI Input version is used (IP4787CZ32).

DESIGN NOTE:
LDO Enable pin function (IP4787CZ32 only):
Low - LDO is disabled (default - external pulldown)
High - LDO is enabled (internal pullup)

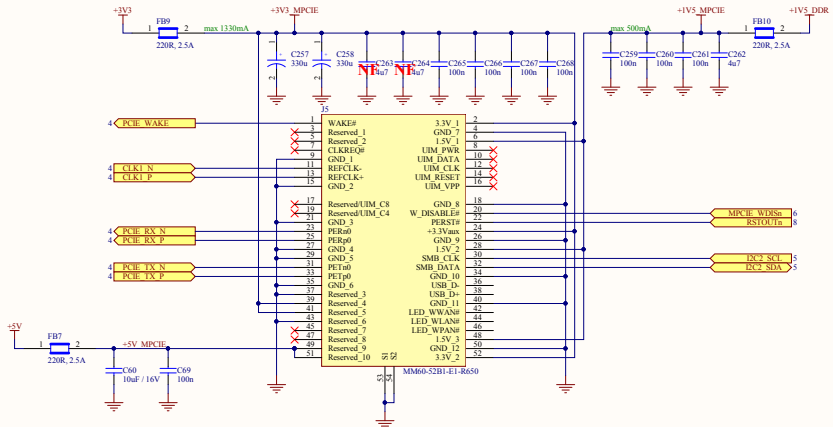
DESIGN NOTE:
E-DDC I2C Address 0x60
DDC2 I2C Address 0xA1

Cannot open file 3D_Robotics_Logo.bmp

Title:	Solo HDTC HDMI	Variant:	[No Variations]
Page Contents:	[12] - HDMI, HDMI OUTPUT.SchDoc		Checked by
Size:	DWG NO		Revision: V4
Date:	2/25/2015	Sheet	12 of 23

PCIE MINI

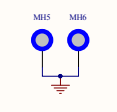
PCIe Mini



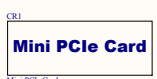
LAYOUT NOTE:
This is a stand off slot. The maximum allowed componenent height in the PCIe Mini Card area is 2.2mm.

LAYOUT NOTE:
Distance between PCIe Mini connector (center of the bigger hole) and mounting hole MH6:
X = 48.05
Y = 0.4mm

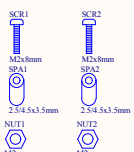
PCIe Card Mounting Holes



PCIe Mini 1 Card for 3D Model



PCIe Card Mounting Accessories

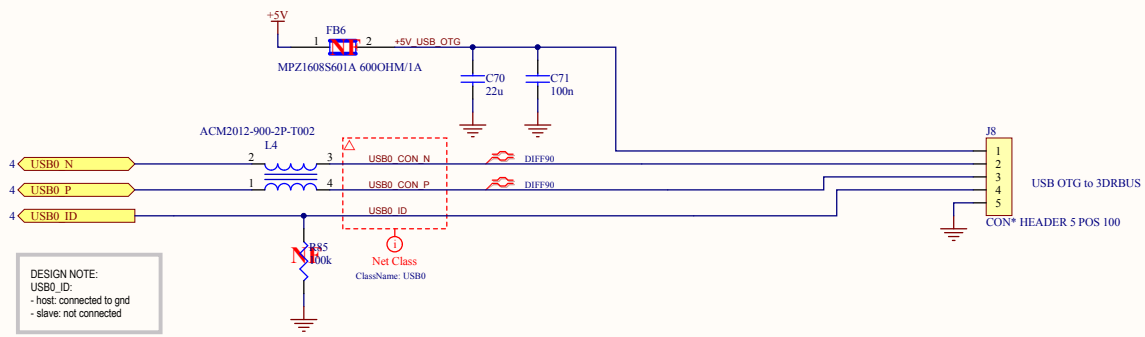


DESIGN NOTE:
The distance between the mounting holes of PCIe Card and the PCB is 3.5 mm.

Cannot open file 3D_Robotics_Logo.bmp

Title:	Solo HDTC HDMI	Variant:	[No Variations]
Page Contents:	[13] - PCIE MINI.SchDoc		Checked by
Size:	DWG NO		Revision: V4
Date:	2/25/2015	Sheet	13 of 23

USB OTG Debug

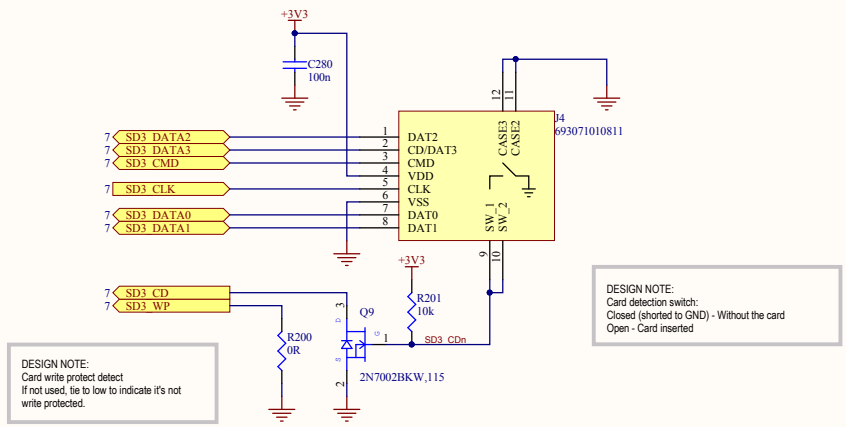


Cannot open file 3D_Robotics_Logo.bmp

Title:	Solo HDTC HDMI	Variant: [No Variations]
Page Contents:	[14] - USB DEBUG.SchDoc	Checked by
Size:	DWG NO	Revision: V4
Date: 2/25/2015	Sheet 14 of 23	

SD CARDS

Micro SD Slot



CR2

Micro SD Card

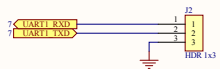
Micro SD Card

Cannot open file 3D_Robotics_Logo.bmp

Title:	Solo HDTC HDMI	Variant:	[No Variations]
Page Contents:	[15] - SD SLOT.SchDoc		Checked by
Size:	DWG NO		Revision: V4
Date: 2/25/2015		Sheet 15 of 23	

UARTS

UART 1 - Debug console (+3V3)



Level translator (3V3 <-> 5V)

Level translator eliminated

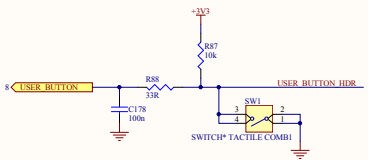
DESIGN NOTE:
Option to use 3V3 or 5V serial ports.

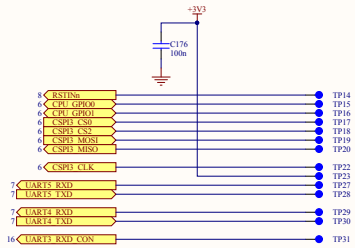
Cannot open file 3D_Robotics_Logo.bmp

Title: Solo HDTC HDMI	Variant: [No Variations]	
Page Contents: [16] - UARTS.SchDoc		Checked by
Size:	DWG NO	Revision: V4
Date: 2/25/2015	Sheet 16 of 23	

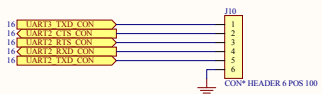
HEADER, SPI, LEDS, EEPROM

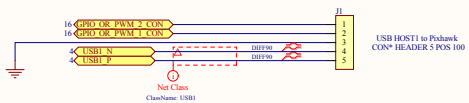
MISC HEADERS



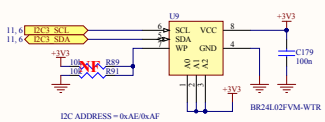


DESIGN NOTE:
Recommendation: To prevent inserting Header J1 the wrong way, we recommend to make the pin 22 as a KEY. Remove/cut out pin 22 from the header and blind the hole in the opposite connector.

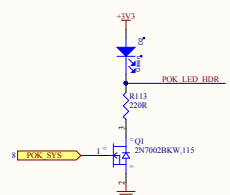




EEPROM

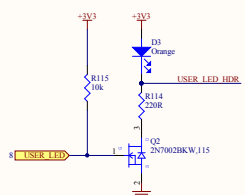


POWER LED



DESIGN NOTE:
Do not fit these LEDs in production.

USER DEFINED LED



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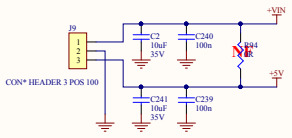
Title:	Solo HDTC HDMI	Variant:	[No Variations]
Page Contents:	[17] - HEADER, SPI, LEDS, EEPROM.SchDoc		Checked by
Size:	DWG NO		Revision: V4
Date: 2/25/2015		Sheet 17 of 23	

POWER INPUT, +3.3V, +1.375V, +3.0_ALWAYS

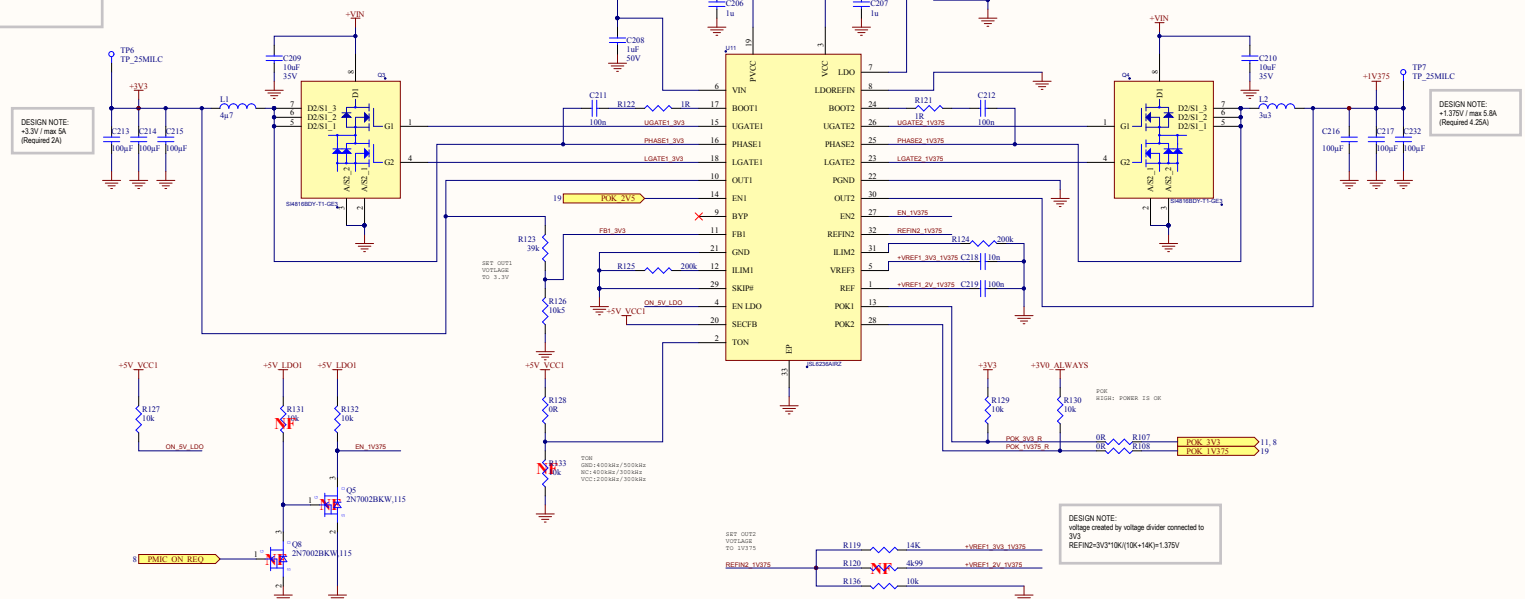
POWER INPUT



DESIGN NOTE:
Option to power the board from 7-24V & 5V (Default) or +5V ONLY

DESIGN NOTE:
Max current 2A per pin

+3V3, +1V375

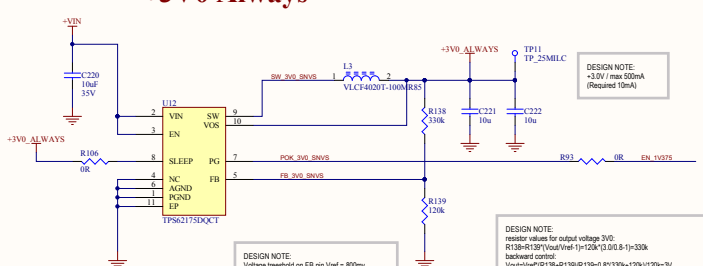


DESIGN NOTE:
+3.3V / max 5A (Required 2A)

DESIGN NOTE:
+1.375V / max 5.8A (Required 4.25A)

DESIGN NOTE:
voltage created by voltage divider connected to 3V3
REFIN2=3V3*10K/(10K+14K)=1.375V

+3V0 Always



DESIGN NOTE:
+3.0V / max 500mA (Required 10mA)

DESIGN NOTE:
Voltage treeshold on FB pin Vref = 800mv

DESIGN NOTE:
resistor values for output voltage 3V0:
R138=R139*(Vout/Vref-1)=120k*(3.0/0.8-1)=330k
backward control:
Vout=Vref*(R138+R139)/R139=0.8*(330k+120k)/120k=3V

Cannot open file 3D_Robotics_Logo.bmp

Title:	Solo HDTC HDMI	Variant: [No Variations]
Page Contents:	[18] - PWR INPUT, 3V3, 1V375, 3V0 ALWAYS.SchDoc Checked by	
Size:	DWG NO	Revision: V4
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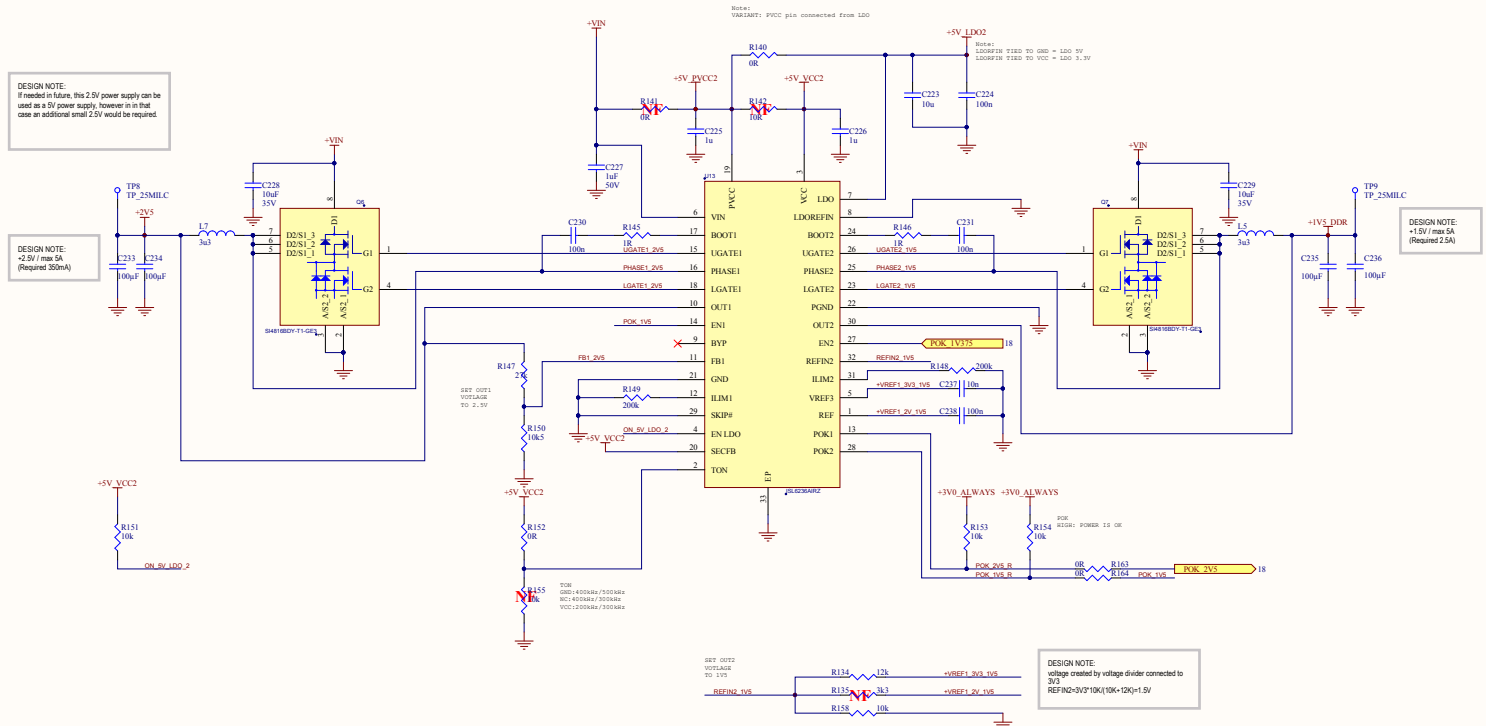
POWER +2.5V, +1.5V

+2V5, +1V5



Cannot open file 3D_Robotics_Logo.bmp

Title:	Solo HDTC HDMI	Variant:	[No Variations]
Page Contents:	[19] - PWR 2V5, 1V5.SchDoc		Checked by
Size:	DWG NO		Revision: V4
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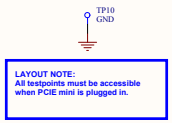
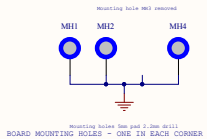
MECHANICAL

TESTPOINT



MOUNTING HOLES



BOARD MOUNTING HOLES - ONE IN EACH CORNER

FIDUCIALS

PCB

Solo HDTC HDMI V1I1 PCB

I2C USAGE AND ADDRESS TABLE

NAME	PERIPHERAL	ADDRESS
I2C1	*On Connector*	
I2C2	*HDMI*	*0x60 , 0xA1*
	HDMI Receiver DDCA (Optional)	*0xA0, 0x74*
	PCIE Mini Card	
I2C3	*HDMI Receiver Control*	*0x98 / 0x99*
	EEPROM	*0xAE / 0xAF*

Cannot open file 3D_Robotics_Logo.bmp

Title:	Solo HDTC HDMI	Variant: [No Variations]
Page Contents:	[20] - MECHANICAL.SchDoc	Checked by
Size:	DWG NO	Revision: V4
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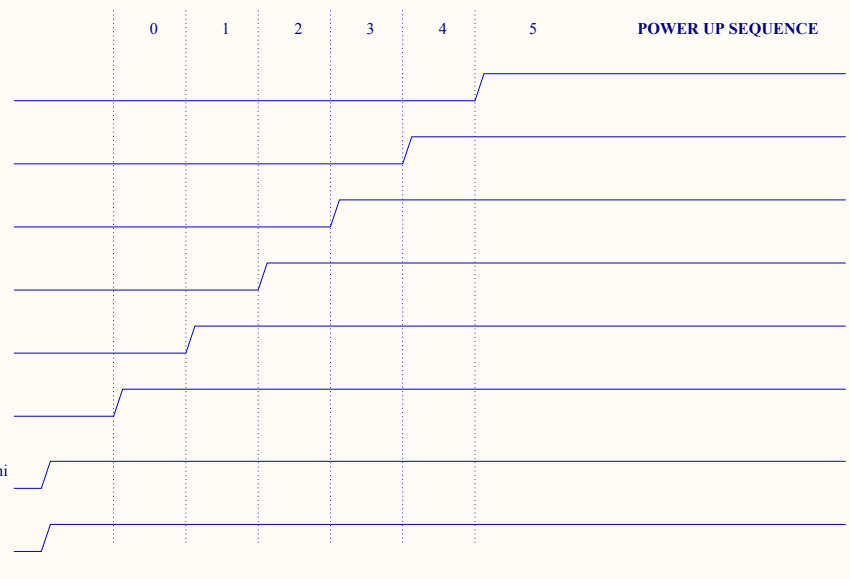
CPU - POWER SEQUENCING

OTHER POWERS	LEVEL	FROM	USED BY
+DDR_VREF	0V75	+1V5_DDR	ref. for DDR memories, gen. with volt. divider
+1V2_VDD_ARM_CAP	1V2	iMX	cpu, core caps
+1V1_VDDSOC_CAP	1V1	iMX	core caps, cpu-sata, cpu-pcie, cpu-hdmi

CONTROLED BY	NAME	LEVEL	USED BY
POK_3V3	+1V8	1V8	HDMI input
POK_2V5	+3V3	3V3	cpu, chips, pull up
POK_1V5	+2V5	2V5	cpu
POK_1V375	+1V5_DDR	1V5	cpu, memory, PCIE mini
EN_1V375	+1V375	1V375	cpu, cpu core voltages
+VIN	+3V0_ALWAYS	3V0	cpu, supervisor, pull up
	+5V	5V	cpu usb, hdmi, 5V uart, PCIE mini
	+VIN	7V-24V	switching power supplies



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Title:	Solo HDTC HDMI	Variant: [No Variations]
Page Contents:	[21] - POWER SEQUENCING.SchDoc	Checked by
Size:	DWG NO	Revision: V4
Date: 2/25/2015	Sheet 21 of 23	

DOC: REVISION HISTORY

HDTC Change V2

August 18, 2014

- Remove: 2mm, 32 position single strip header.
- Add: 2.54mm, 6 position header J10 (UART).
- Add: 2.54mm, 5 position header J1 (USB H1, 2x GPIO).
- Add: 2.54mm, 5 position header J8 (USB OTG).

August 19, 2014

- Remove: USB H1 connection from J5. PCIe does not require USB.
- Remove: uUSB connector. All updates through 802.11
- Add: SW1 momentary tactile switch.
- Add: USB OTG connection to J8.
- Add: USB H1 connection to J1.

HDTC Change V3

September 6, 2014

- Remap: Ball N3, N4, N5, N6 from U1N to U1O
- Remap: Ball H21, J20 from U1E to U1O
- Remap: AUD3 function is replaced with AUD4_TXC, TXFS, RXD (U22, V24, W24).
  Remap AUD3_TXC ball N1 <<>> AUD4_TXC ball U22.
  Remap AUD3_TXFS ball N4 <<>> AUD4_TXFS ball V24.
  Remap AUD3_RXD ball N3 <<>> AUD4_RXD ball V24.
  Keep AUD3_CLK on same ball T5. Renamed only to AUD4_CLK.
- Remap: USB_H1_OC ball J20 to GPIO3 ball R7
- Remove: I2C1 (H21 and J20), pads are now used for DAT02 and DAT03

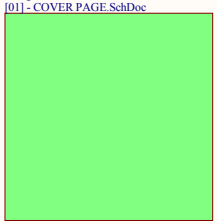
September 7, 2014

- Remove: U8 Level translater
- Remove: R84, R95, R86
- Remove: C72, C175, C181
- Remove: VID_IN_CSI0_VS/FIELD net and port from U1O and U4
- Remove: VID_IN_CSI0_HS net and port from U1O and U4
- Remove: VID_IN_CSI0_INT1 net and port from U1O and U4
- Remove: VID_IN_CSI0_INT2 net and port from U1O and U4
- Remove: VID_IN_CSI0_DE net and port from U1O and U4

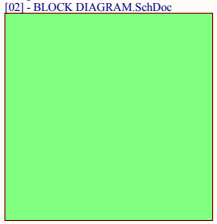
Cannot open file 3D_Robotics_Logo.bmp

Title:	Solo HDTC HDMI	Variant:	[No Variations]
Page Contents:	[22] - DOC REVISION HISTORY.SchDoc	Checked by	
Size:	DWG NO	Revision:	V4
Date: 2/25/2015	Sheet 22 of 23		

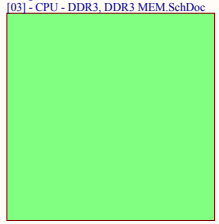
Designator
[01] - COVER PAGE.SchDoc



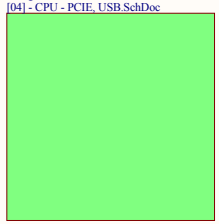
Designator
[02] - BLOCK DIAGRAM.SchDoc



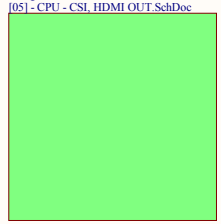
Designator
[03] - CPU - DDR3, DDR3 MEM.SchDoc



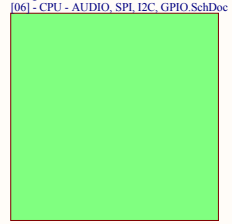
Designator
[04] - CPU - PCIE, USB.SchDoc



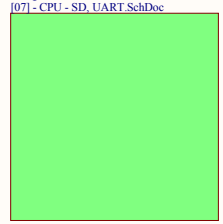
Designator
[05] - CPU - CSI, HDMI OUT.SchDoc



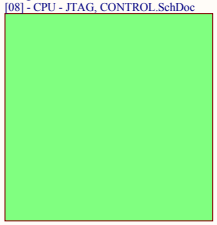
Designator
[06] - CPU - AUDIO, SPI, I2C, GPIO.SchDoc



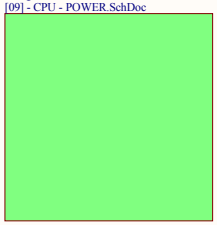
Designator
[07] - CPU - SD, UART.SchDoc



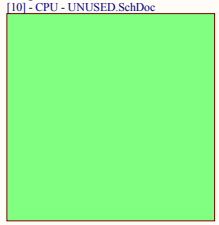
Designator
[08] - CPU - JTAG, CONTROL.SchDoc



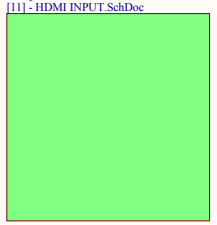
Designator
[09] - CPU - POWER.SchDoc



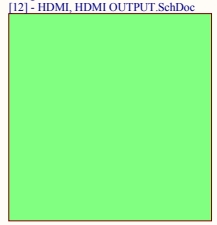
Designator
[10] - CPU - UNUSED.SchDoc



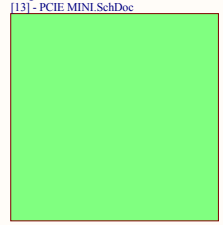
Designator
[11] - HDMI INPUT.SchDoc



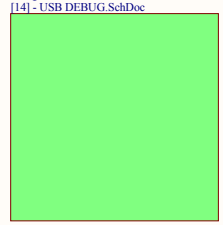
Designator
[12] - HDMI, HDMI OUTPUT.SchDoc



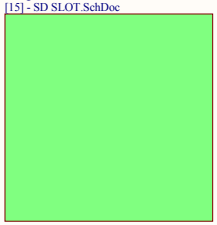
Designator
[13] - PCIE MINI.SchDoc



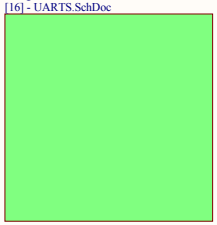
Designator
[14] - USB DEBUG.SchDoc



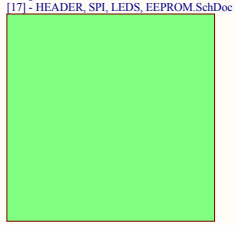
Designator
[15] - SD SLOT.SchDoc



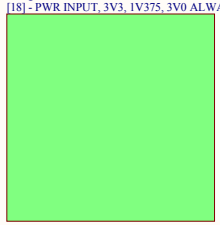
Designator
[16] - UARTS.SchDoc



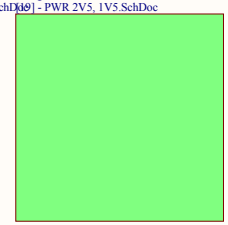
Designator
[17] - HEADER, SPI, LEDS, EEPROM.SchDoc



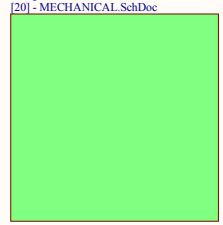
Designator
[18] - PWR INPUT, 3V3, 1V375, 3V0 ALWAYS.SchDoc



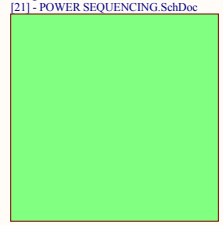
Designator
[19] - PWR 2V5, 1V5.SchDoc



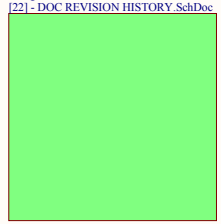
Designator
[20] - MECHANICAL.SchDoc



Designator
[21] - POWER SEQUENCING.SchDoc



Designator
[22] - DOC REVISION HISTORY.SchDoc



NOTES

Mark Not Fitted Components as
NF

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

Cannot open file 3D_Robotics_Logo.bmp

Title: Solo HDTC HDMI		Variant: [No Variations]
Page Contents: Solo HDTC_HDMI_REV_A Project.SchDoc		Checked by
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